Neeraj Prabhu

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Education

University of Utah *[Aug 2024 - Present]*
Doctor of Philosophy | Computer Science

Indian Institute of Technology Bombay (IITB) *[Nov 2020 - May 2024]*
Bachelors of Technology | Department of Electrical Engineering GPA: 8.82/10
Major in **Electrical Engineering** (with honors), and a minor degree in **Computer Science**

Research Experience

Graduate Research Assistant | University of Utah *[Aug 2024 - Present]*
Advisor: Prof. Rajeev Balasubramonian

- Researching various cryptographic techniques to facilitate efficient memory integrity verification
- Exploring the advantages of processing-in-memory to optimize the performance of bilinear accumulators for memory integrity verification, reducing the overhead of fetching MACs and integrity trees
- Conducted an extensive literature survey to understand the various operations in zero knowledge proof systems and look into opportunities for hardware acceleration techniques for different systems

Research Intern | Utah Arch Group *[May 2023 - July 2023]*
Advisor: Prof. Rajeev Balasubramonian

- Characterized FHE operations implemented in the **Microsoft SEAL** library using **Intel VTune** and **Perf**
- Generated **roofline plots** for multiple workloads using FHE operations and analyzed the memory-access instructions, compute instructions, and last-level cache accesses to identify that FHE is **memory-bound**
- Implemented addition, multiplication—including **key switching**, rescaling, **NTT** transforms—and rotation in the CKKS scheme on **UPMEM** by parallelizing them on several DPUs to improve performance
- Conducted extensive literature survey regarding FHE to understand optimization techniques used in state-of-the-art **FHE accelerators** and studied the architecture of **UPMEM PIM** to correlate the two

Research Assistant | CADSL, IIT Bombay *[July 2023 - Dec 2023]*
Advisor: Prof. Virendra Singh

- Analyzed the use of **STTRAM** for BTBs and the performance benefits with the faster read accesses
- Implemented **BTB-X** on **ChampSim** and compared its performance with a conventional BTB along with an analysis of BTB **MPKI**, **memory footprint**, branches stored, and power requirements
- Surveyed existing literature regarding different **BTB organizations** and ways to reduce the size of BTBs

Research Assistant | P-Quest Lab, IIT Bombay *[Jan 2023 - May 2024]*
Advisors: Prof. Kasturi Saha, Prof. Laxmeesha Somappa

Realtime Bayesian ODMR on Xilinx ZCU111

- Designed an FPGA-based **Bayesian inference** technique to reduce the time required for the completion of ODMR with **on-board estimation** of the intensity, and feedback to generate the excitation signal
- Implemented the algorithm consisting of a **random number generator**, a computation unit to update the weights of the sampling points, and a selection unit to minimize the number of samples required
- Integrated custom Verilog code with the **Zynq MPSoC** and **RFSoC IPs** to generate microwave signals

FPGA-based photon correlator

- Simulated a photon correlator on Xilinx Vivado using the **multi-tau correlation** technique to accommodate large experiment times while avoiding the use of a large number of correlation channels
- Designed and integrated an input sampler, **clock divider**, and an **accumulator** to form the correlator
- Obtained a **Poissonian distribution** of photon strikes with a timing resolution of approximately 200ps

Awards And Accolades

- Acheived **All India Rank 207** in the JEE-Advanced Exam, out of over 0.15 million candidates *[2020]*
- Secured **All India Rank 691** in the JEE-Mains Examination, out of over 800 thousand candidates *[2020]*
- Qualified for **INChO** by securing a rank in the **top 802** in NSEC *[2020]*
- Selected for the prestigious **KVPY** (Kishore Vaigyanik Protsahan Yojana) fellowship *[2020]*
- Awarded a **Best Project Award** for our design of a fluxgate sensor & lock-in amplifier in EE 344 *[2023]*

Technical Projects

Implementation of Freeflow Core on GEM5 *[Sep 2023 - Dec 2023]*

Advanced Topics in Computer Architecture (EE748) | Prof. Virendra Singh

- Conducted extensive literature survey regarding techniques to optimize the performance of in-order cores by exploiting **memory level parallelism** while maintaining a low power budget
- Implemented **multiple queues** before the dispatch stage to separate **memory access** and **address-generating** instructions which will be identified using a backward propagation algorithm

Lock-in Amplifier with flux-gate sensor *[Jan 2023 - Apr 2023]*

Electronics Design Lab (EE 344) | Prof. Siddharth Tallur, Prof. Kasturi Saha, Prof. Laxmeesha Somappa

- Designed a flux-gate sensor from scratch using **in-house components**, which included the design of a printed circuit board (PCB) and optimization of **coil parameters**, all in a ready-to-go package
- Integrated a Red-Pitaya lock-in amp with the flux-gate sensor for **real-time sensing** of DC magnetic fields

Superscalar Microprocessor Design *[Aug 2022 - Nov 2022]*

Advanced Computer Architecture (CS 683) | Prof. Virendra Singh

- Designed a **2-way fetch Out-Of-Order** superscalar microprocessor using **6-stage pipelines** with a **128-entry reservation station** and a **256-entry reorder buffer**
- Developed a **2-bit branch predictor** and hardware to **resolve incorrect branches** after execution

Accelerating VLSI CAD Algorithms *[Jan 2023 - Apr 2023]*

Parallel Scientific Computing and Visualization (AE6102) | Prof. Prabhu Ramachandran

- Improved the performance of **graph algorithms** used in VLSI circuit design and analyzed the results, comparing the time for multiple graph sizes against Python libraries such as **pyEDA** and **NetworkX**
- Achieved a performance benefit of the order of **100x** for large graphs using **numba accelerated** versions of graph algorithms (shortest path, minimum spanning tree) over the networkx implementation

View other projects on my website [link]

Positions Of Responsibility

System Engineer | Student Satellite Program, IIT Bombay *[Oct 2022 - Sep 2023]*

A 50+ member student team with the vision of making IIT Bombay a centre of excellence in space technology, working on developing various CubeSat-compatible modules and an automated ground station

- Part of the leadership group of a multi-disciplinary team of **50+ students** across 4 projects with **INR 2.8M** annual budget and assigned the responsibility of managing the **ham radio club** of the institute
- Restructured the team's **leadership structure** and adopted a technical approach emphasising iterative **hardware prototyping and testing**, resulting in increased efficiency and faster project completion

Department Academic Mentor (DAMP Mentor) *[May 2023 - Apr 2024]*

DAMP Cabinet, Student Mentorship Programme, IIT Bombay

- Selected into a team of **46 members** out of **100+ prospects** on the basis of **rigorous interviews** to help **6 sophomores** strike a balance between academics and extracurricular activities
- Selected as a senior DAMP Mentor to help academically weaker students improve their academic standing

Teaching Assistant *[Jan 2023 - May 2023]*

EE 309: Microprocessors | Prof. Virendra Singh

- Entrusted with the responsibility of being a teaching assistant for the sophomore year course EE 309
- Conducted sessions for **50+ students** to recap the course contents and attend to doubts

Technical Skills

Programming Languages	C++, Verilog, VHDL, Embedded C, Python, MATLAB
Libraries	Numba, MPI4PY, Automan, Mayavi, SciPy, Pynq, NumPy, Pandas, Scikit-learn, Tensorflow, OpenCV, PyRPL
Software	GEM5, ChampSim, GPGPU-Sim, Vivado, Vitis, Intel Pin, Intel VTune, Perf, Ansys HFSS, EAGLE, NGspice, GNU-Radio

Extra-Curricular Activities

- Completed **80+ hours** of volunteering service in the **Green Campus** department of **NSS, IIT Bombay**
- Satellite Tracking
  - Tracked the **ISS** and received **SSTV** images during the **ARISS event** using a Yagi Antenna
  - Tracked the **NOAA** Satellites and received **weather images** using an in-house Egg-Beater Antenna
- Conducted a day-long workshop to help 80+ participants from various institutes setup their ground stations